Journal of Instrumentation

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PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 19, 2012*
ACCEPTED: *November 28, 2012*
PUBLISHED: *January 15, 2013*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2012,
17–21 SEPTEMBER 2012,
OXFORD, U.K.

Performance of the NA62 LAV front-end electronics

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ABSTRACT: The NA62 experiment [1] will measure the BR($K^+ \to \pi^+ \nu\bar{\nu}$) to within about 10%. To reject the dominant background from final state photons, the large-angle vetoes (LAVs) must detect particles with better than 1 ns time resolution and 10% energy resolution over a very large energy range. A low threshold, large dynamic range, Time-over-threshold based solution has been developed for the LAV front end electronics. Our custom 32 channel 9U board uses a pair of low threshold discriminators for each channel to produce LVDS logic signals. The achieved time resolution obtained in laboratory, coupled to an HPTDC based readout board, is ∼150 ps.

KEYWORDS: Analogue electronic circuits; Modular electronics; Front-end electronics for detector readout; Trigger algorithms

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doi:10.1088/1748-0221/8/01/C01020

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1 The NA62 large angle veto detector

The large angle veto detector is made by 12 stations of different radii, ANTI-A1 to ANTI-A12, to assure an angular coverage for photons between 8-50 mrad [2] . The first eleven stations are part of the vacuum decay tube, while the last is located outside the vacuum tank. There are 4 different types of veto station whose characteristics are listed in table 1. In figure 1 the ANTI-A1 station is shown. Each type has a different number of layers, 4 or 5, of lead glass blocks, coming from the dismantled electromagnetic calorimeter of the OPAL experiment.

The layers are staggered in azimuth providing complete hermeticity of at least three blocks in the longitudinal direction. The blocks, made of Schott SF57 lead glass (see figure 1), have the shape of a truncated prism with different shapes and dimensions (with minimal variations between different types) . The block length is always 370 mm. One of the square faces of the lead glass has a 1 cm-thick steel flange glued to it. This flange has four threaded holes for fixing the counter to the support bracket, one for the connection of a calibration diode, and a central large hole for the passage of a cylindrical light guide for light collection. The light guide is a cylinder of SF57 lead glass with a diameter of 76 mm and a height of 40 mm. It is glued to the lead glass block and, at the other end, to a Hamamatsu R2238 photomultiplier. An external mu-metal shield, enclosing the guide and the PM, is glued to the steel flange.

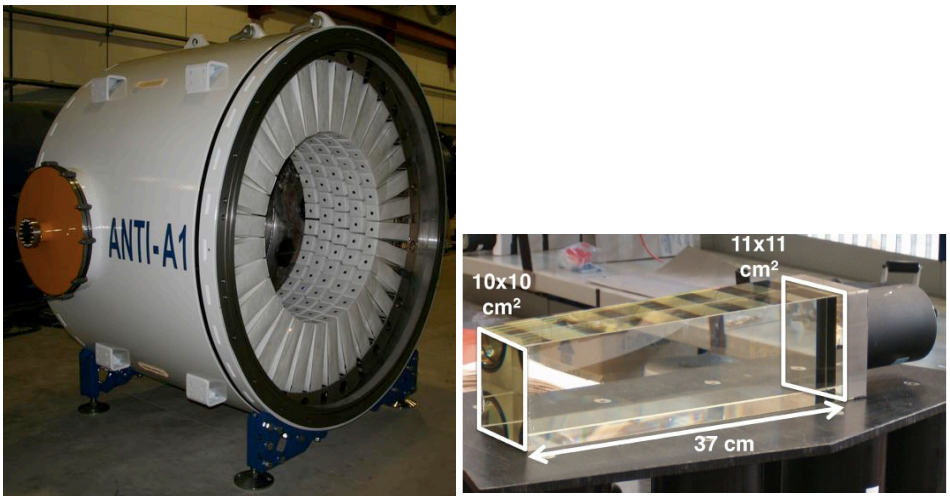

Figure 1. The complete ANTI-A1 station (left) and an opal lead glass block (right).

Table 1. LAV stations description.

Station number	Inner diameter	Outer diameter	# layers	# blocks	# of RO ch
A1-A5	1073 mm	1813 mm	5	160	320
A6-A8	1534 mm	2274 mm	5	240	480
A9-A11	1960 mm	2700 mm	4	240	480
A12	2144 mm	2884 mm	4	256	512
total				2496	4992

2 LAV readout

The LAV system will mainly detect photons from kaon decays, as well as muons and pions in the beam halo. For each incoming particle the veto detectors are expected to provide a time measurement with 1 ns resolution and an energy measurement with a moderate precision (of order 10%). The system should be able to operate with thresholds of few millivolts, well below the minimum-ionising-particle (MIP) signal, in order to keep the detection efficiency for muons and low energy photons as high as possible. Because of the intrinsic time resolution of the lead-glass blocks (¡1ns) and the rise time of the Hamamatsu R2238 PMT (5 ns), the requirements are not stringent on the time measurement accuracy. On the other hand, the expected energy deposit in the LAV stations from photons coming from π^0 decays covers a very wide range, from 10 MeV up to 30 GeV. Using the measured average photoelectron yield of 0.3 p.e./MeV and a nominal gain of $1 \cdot 10^6$ for the R2238 PMT, one expects a 4.5 pC charge for a MIP, corresponding to a signal amplitude of 20 mV on a 50Ω load. On the upper part of the range, signals from 20 GeV showers can reach an amplitude of 10V for a 50Ω load. The readout for the LAV stations consists of two different types of boards (see figure 2): a dedicated front end card developed for the LAV detector, and a common digital readout board called TEL62, used by most of the NA62 detectors. The LAV front

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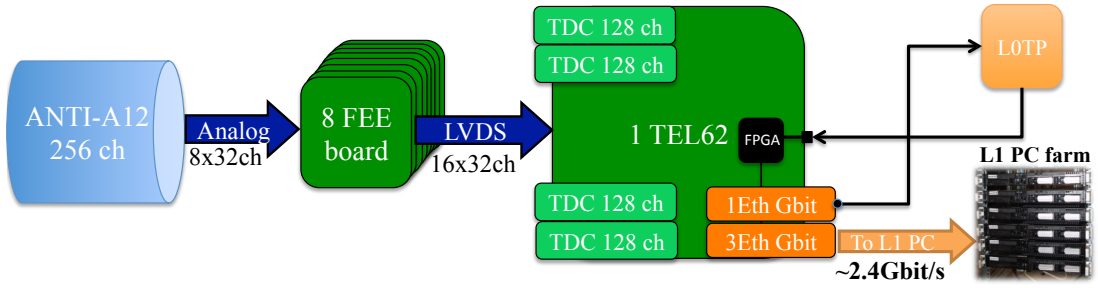

Figure 2. The LAV readout scheme. The ANTI-A12 station has been used as example.

end board converts the analogue input coming from the PMT into an LVDS digital signal using two comparators with different threshold on each channel. The duration of each of the LVDS pulses is equal to the time the analogue signal is over the programmed threshold. The LVDS logic signals are sent to the readout board TEL62 in which a custom designed TDC mezzanine converts each signal in digital leading and trailing times. The TEL62 on-board FPGAs are used to correct raw hits times and to produce a L0 trigger primitive (see 6) to be sent to the L0 trigger processor using a dedicated Gbit ethernet interface. On a positive L0 trigger request the TEL62 sends the data to the L1 PCs using the remaining 3x1Gbit ethernet interfaces. The system has $\sim$ 2500 analogue input channels and $\sim$ 5000 digital readout channels in total. The system in expected to sustain rates of physical particles up to 100KHz per channel and to produce a data volume to the L1 PC farm lower than 2.4 Gbit/s for each stations.

3 The LAV front end electronic board

The LAV front end board is implemented on a 9U VME standard layout with the J1 power connector only at the top of the backplane side. No VME bus line is connected to the board, only customs $\pm$ 7.5 V power lines are used. At the bottom the 32 analogue inputs are connected to the board using two DB37 connectors (see figure 3). Each single input produces two different outputs due to the presence of two programmable thresholds on each channel. The resulting 64 LVDS digital outputs are connected to the TDC using two SCSI2 connectors placed on the front panel of the board. The analogue sums of 4 and 16 channels are provided on 8 + 2 LEMO00 connectors for monitoring of the analogue signal. The communication and the threshold setting are managed by the CAN-Open protocol through two RJ-45 connectors. To simplify maintenance and reduce costs, the board has a modular structure. The 9U motherboard manages input, output and power distribution while the rest of the functionalities are implemented on 4 types of mezzanine described in the following.

3.1 Board controller mezzanine

The LAV front end card is not equipped with a VME interface and the remote control of the board is obtained using a CPU. The board controller mezzanine is responsible for the communication with the slow control PC and for the settings of the 64 thresholds of the comparators. It is based on the C8051F040 CPU, and communicates through the CAN-Open protocol and allowing different operations to be performed. The slow control functionality includes the monitoring of the low

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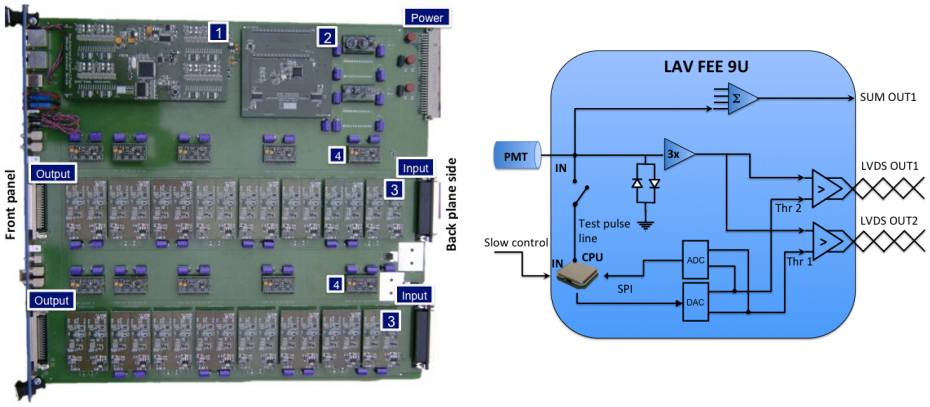

Figure 3. The LAV front end board (left) and its block diagram (right).

voltage power lines and the measurement of the board temperature. The board also communicates with the time over threshold (described in section 3.3) mezzanine allowing the threshold of each comparator to be set and read, and with the pulse generator mezzanine (described in section 3.2 allowing to set the value of the pulse height and frequency and the pattern of channels to be pulsed.

3.2 Test pulse generator mezzanine

For use in the diagnosis of the functionality of the electronics, channel mapping, channel integrity and threshold calibration, the design of the board includes an internal pulse generator. The pulse generator is able to provide pulses with 5-50 ns programmable width and 50-250 mV programmable amplitude using 12-bit words. The stability of both amplitude and width is of the order of 3% and the pulse rise time is $\sim$2 ns. The internal pulser can be triggered both locally, controlled by the on board CPU, or externally using an external signal coming from TEL62. To allow maximum flexibility, the pattern of channels to be pulsed can be programmed. The pulse signal is directly sent to the input connectors. Exploiting the high impedance of the signal input line from the PMT voltage divider, as well as the fact that the pulser signal travels both in the detector direction and the comparator direction, by measuring the characteristics of the reflected pulse, the integrity of cables and connection of all the electronic chain can be checked.

3.3 Time over threshold (ToT) mezzanine

This is the core part of the LAV FEE which operates on the analogue signal to produce the LVDS output. The LAV FEE board houses 16 of these mezzanines which are able to manage 2 input channels each. The most important part of one single channel is described in figure 4. Just after the input connection the signal is divided into two copies using a passive resistive splitter. One copy is sent to the circuit responsible for the sums while the other is sent to the ToT chain. In order to avoid channel saturation by the input signals, the input amplitude must be limited to a maximum of 600 mV. The clamping circuit is designed to be able to sustain high rate of signal up to 10 V, but is able to tolerate even larger isolated signals. To preserve the ToT measurement, the circuit must clamp the signal without changing its time duration. This is achieved by an active clamp using a pair of very fast low capacitance diodes (D25 in figure 4) and an amplifier (U10) (see pag. 203 in ref. [1]).

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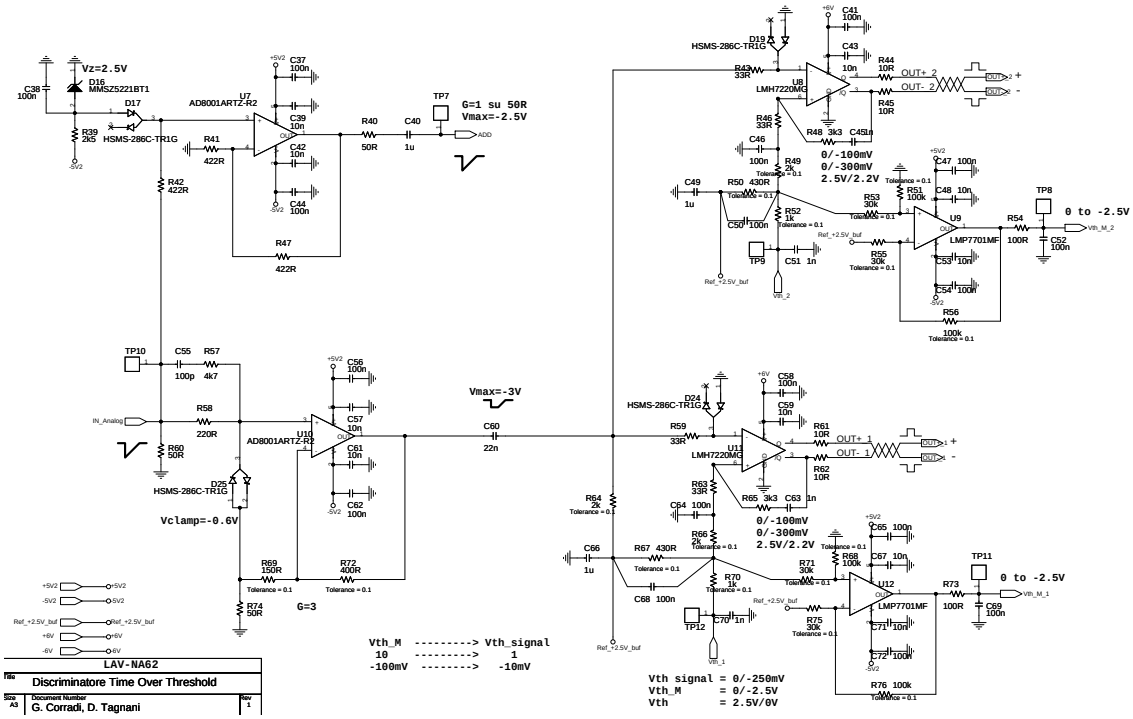

Figure 4. Time over threshold circuit single channel layout.

The ToT system must work with an effective threshold, of a few mV on the analogue signal in order to maximise efficiency. To improve signal to noise separation and reduce the walk dependence on the analogue amplitude (overdrive), a moderate amplification is needed. A gain of 3 was chosen, never the less it can be modified with ease (up to 5) in future by adding an SMD resistor. A very low noise, high bandwidth (800 MHz), high speed Current Feedback Amplifier (AD8001, U10 in figure 4) is used for this purpose. After a decoupling capacitor, to suppress amplifier DC offset the output is sent to the comparator input. The amplified signal is picked up at high impedance by two LMH7220 High Speed Comparators with LVDS drivers (U8 and U11). These devices compare the input with programmable thresholds which can be adjusted in the range 5-250 mV with a 12 bit resolution using the DAC in the board controller mezzanine. The LMH7220 has only a 2.5 ns propagation delay and 0.6 ns rise and fall times on the LVDS signal, minimising the impact on the TDC performance. To reduce noise-induced double pulses at the comparator output, a $\sim$3 mV hysteresis is also provided through a feedback resistor. The comparator produces an output signal starting when the leading edge of the analogue signal crosses the threshold, and stopping when the trailing edge crosses the threshold again. This digital signal is transmitted to the TDC using the LVDS differential standard. To dump the effect of impedance mismatch a pair of output resistors are used on the LVDS lines.

3.4 Analogue sum mezzanine

In order to have the possibility to monitor the input analogue signals to the FEE board, an analogue output is required. Due to mechanical constraints it is impossible to duplicate all 32 analogue inputs on LEMO connectors on the front-panel. The analogue input signals are therefore collected in sums

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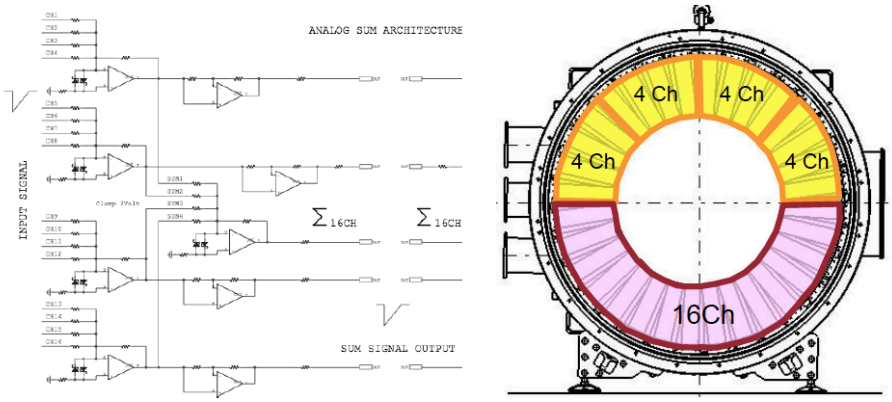

Figure 5. Analogue sum layout. On the right side the geometry of sums on the smaller ANTI, e.g. A1 to A5.

of four blocks (one azimuth segment) by means of one analogue sum mezzanine. Afterwards they are summed again in groups of four to get a sum of 16 blocks through one more mezzanine. In the end, every 9U board contains 10 sum mezzanines. Each sum mezzanine has a gain of 0.5 (resulting in a gain of 0.25 for the sum of 16 blocks), nevertheless the inputs of each sum are clamped at 600 mV before the summation (see figure 5). The FEE board front panel is equipped with 8 LEMO connectors for the sums of 4 blocks, (in yellow in figure 5), and two LEMO connectors for the sums of a 16 blocks, (in violet in figure 5). Using a QDC, the total charge on 4 or 16 channels can be measured.

4 Testing LAV front-end boards

In order to test and characterise all the LAV FEE boards, an automatic test stand has been set up at Laboratori Nazionali di Frascati (LNF).

4.1 Test setup

A pulse generator (Agilent 81110A) was used to generate test signals having a variable height and a fixed rise time of 5 ns and a fall time of 16 ns. The generated signal was passively split into 32 copies and fed into the input DB37 connectors of one LAV FEE board. All the copies of the signal were proven to be equal within 2%. The 64 LVDS outputs were connected to a VME commercial board (CAEN V1190B) housing the HPTDC chip, the same TDC ASIC as the actual TEL62 readout. Digital data was collected through a VME controller (CAEN V1718) and stored on a PC. The PC was as well programmed to configure front-end threshold values through USB and the pulse generator, through GPIB, to change the signal amplitude in such a way that an automatic procedure was established. The complete test of one LAV FEE board took about 15 minutes.

4.2 Test results

Two kinds of measurements were performed on the boards: minimum threshold and time resolution. For the former, the amplitude of the input signal was varied in the range from 5 mV up to 20 mV. The threshold was set to the nominal value of 2 mV. This was the lowest value at which the

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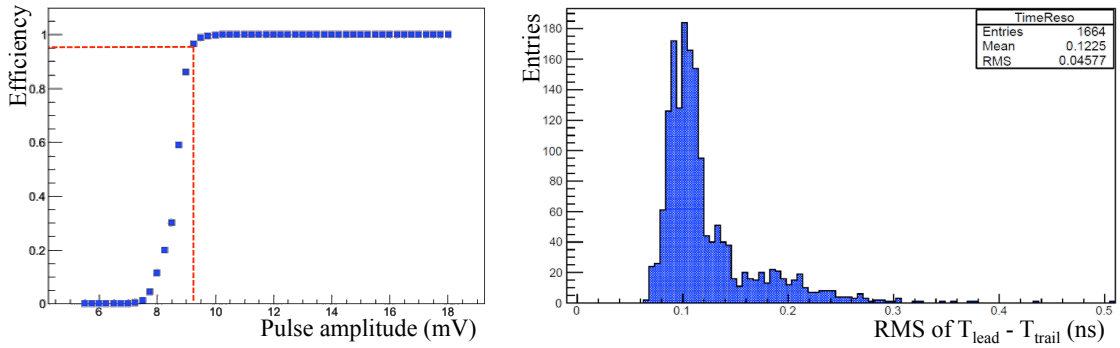

Figure 6. On the left: a plot of the threshold profile. On the right: the distribution of the RMS of repeated time measurement of a probe signal, performed with every channel. The probe signal has amplitude of 100 mV and fixed width of 30 ns within 40 ps RMS.

noise rate was less than 100 Hz on each channel. In the meantime the efficiency of each channel was measured as the number of delivered pulses divided the number of detected pulses. Results from this measurement are reported in the left plot of figure 6. The minimum threshold was defined to be extrapolated at the level 95% efficiency, as shown in figure by red dashed lines. As far as the time resolution is concerned, we performed a repeated measurement of the difference in time between the leading and the trailing edge of the input signal. This is set by the pulse generator to a value of about 30 ns and its variation was proven to be less than 40 ps by means of repeated measures performed through a digital oscilloscope. We therefore evaluated the root mean square (RMS) of the time-difference distribution. These RMS values, for the all the channels of 26 boards, are represented in the right plot in figure 6. One can see that most of the channels have a time resolution of the order of 100 ps. The long tail on the right of the plot is due to some noisy channels that are still under study. Nevertheless the performance could be increased by replacing the noisy ToT mezzanines, thanks to the modularity of the design.

5 Simulation

In order to better understand detector and electronics performance a detailed Monte Carlo simulation has been developed for the digitisation procedure [3]. In the simulation, the number of photons on the PMT photocathode their energies and arrival times are obtained from GEANT4 NA62 official Monte Carlo. The behaviour of the R2238 PMT is then simulated including the photocathode quantum efficiency as a function of the wavelength, the multiplication process in the 12 dynodes, the output RC circuit, and the cables. The simulated PMT signal is then processed by the simulation of the front end which, taking into account thresholds and hysteresis, produces the value of the simulated leading and trailing times. To validate the simulation, the curve of time over threshold vs charge has been compared with test beam data: a very good agreement with the data is achieved over a range of charge going from a few pC up to 100 pC.

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6 LAV trigger-generating firmware

The digital readout of the all the detectors participating to the NA62 experiment is based on the TEL62 board [4] which collects the data coming from TDCs and transfer them through a gigabit ethernet when a trigger signal is received. Some detectors, among which the LAV, must at the same time generate the so-called L0 trigger primitive, i.e. the value of the time at which some specific physics event occurred. In order to do that many detector-specific firmwares must be designed.
As far as LAV is concerned, the event on which a trigger primitive must be generated is simply the signal crossing both the high an the low thresholds on the same block. At the aim of finding these events and producing the proper trigger primitives a LAV-specific trigger generating firmware was developed. It consists of a independent data-stream parallel to the data one. As a first step events are distributed among different FIFOs, one for each high threshold and low threshold channel. While the FIFOs are filled, a finite state machine search for an event, i.e. for the crossing of high and low threshold in the same block. Once the association is performed, the resulting event time is corrected for the slewing (or time-walk) error, according to the following formula:

$$t = t_{\text{low}} - \frac{(t_{\text{high}} - t_{\text{low}}) \cdot t_{\text{low}}}{V_{\text{high}} - V_{\text{low}}}$$

where V_{high}, V_{low} are the high, low threshold voltages and t_{high}, t_{low} are the respective crossing times. At last events occurring within a specific time window (programmable up to $\sim$ 25 ns) are grouped together to form a cluster whose time is calculated as the average of single times. At last the time values of the clusters are sorted and delivered to the last firmware block to build the trigger primitives and send them to the L0 trigger processor.

7 Conclusions

A low cost, large dynamic range, time-over-threshold based solution has been developed for the LAV front end electronics. An automatic test station has been built at LNF and $\sim$30 boards have been characterised and are now up and running at the NA62 experimental site. The achieved time resolution has been measured to be of the order of 100 ps for most of the electronic channels, while the minimum effective threshold has been proven to be less than 10 mV. The LAV-specific primitive-generating firmware has been developed and tested on the TEL62 boards with promising results.

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